Declaration

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Osaka, this 22nd day of August, 2007

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[Attached Documents]

[Name of Document]	Specification	1
[Name of Document]	Drawing	1
[Name of Document]	Abstract	1
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[Name of the Document] Description

[Title of the Invention] Semiconductor integrated circuit

[claims]

[claim 1] A semiconductor integrated circuit including:

pads, and

wirings which are electrically connected to the pads,

wherein said wirings are connected to bumps of a probe card, in an area other than an area where the pads are disposed.

[claim 2] A semiconductor integrated circuit as defined in Claim 1 wherein

at least two of said wirings contact one of said bumps, without being in touch with each other.

[claim 3] A semiconductor integrated circuit as defined in Claim 2 wherein

said wirings have a shape so that an area contacts said bump is broader than a linear shape.

[claim 4] A semiconductor integrated circuit as defined in Claim 2 wherein

said wirings have separable portions.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a semiconductor integrated circuit such as a LSI, and more particularly, to wafer level burn-in for the semiconductor integrated circuit.

[0002]

[Background Art]

A plurality of semiconductor integrated circuits such as LSIs fabricated on a semiconductor wafer are subjected to an acceleration test (burn-in) for detecting initial failures before shipping. In this burn-in, an aging test is carried out at a high temperature (about 120~150℃) for a few hours.

[0003]

Currently, a method of performing burn-in simultaneously on plural semiconductor integrated circuits in a wafer (wafer level burn-in) is proposed (e.g., Japanese Published Patent Application No. 2001-93947). When wafer level burn-in becomes practicable, burn-in can be carried out before packaging, whereby a reduction in cost for burn-in, such as a reduction in the number of failures to be packaged, can be expected.

[0004]

Hereinafter, conventional wafer level burn-in will be described with reference to figures 1 to 3. As shown in figure 1, plural semiconductor integrated circuits 2 such as LSIs are provided on a semiconductor wafer 1. As shown in figure 2, in each semiconductor integrated circuit 2, plural pads 4 are disposed on the periphery of a function circuit 3. When performing wafer level burn-in, it is necessary to apply a current to the plural pads 4. Therefore, bump contact areas 5 are provided on the respective pads 4, and plural bumps 6

provided on a probe card 7 are brought into contact with the bump contact areas 5 as shown in figure 3, to apply a current to the pads 4. Thereby, the semiconductor integrated circuits 2 in the wafer can be subjected to burn-in.

Patent Document 1: Japanese published patent application no. 2001-93947

Patent Document 2: Japanese patent application no. Sho.52-67741

[0005]

As described above, when performing wafer level burn-in to the conventional semiconductor integrated circuits, it is necessary to bring the bumps of the probe card into contact with the plural pads on the plural semiconductor integrated circuits disposed on the semiconductor wafer. As for the bumps of the probe card to be used for wafer level burn-in, there is a restriction that a predetermined interval between bumps must be secured. If the predetermined interval is not secured, no bumps can be fabricated. As a result, wafer level burn-in cannot be accurately performed. Therefore, when the number of semiconductor integrated circuits per wafer is increased with a reduction in the chip area of each semiconductor integrated circuit, the number of bumps per semiconductor integrated circuit chip must be decreased. Therefore, when the chip area of each semiconductor integrated circuit is reduced, it is impossible to fix all of the pads of the semiconductor integrated circuits on the semiconductor wafer by the bumps. As a result, wafer level

burn-in cannot be carried out.

[0006]

Accordingly, the present invention has for its object to provide a semiconductor integrated circuit on which wafer level burn-in can be carried out even when the chip area thereof is reduced.

[0007]

[Disclosure of the Invention]

[Problems to be solved by the Invention]

In order to solve the above-mentioned problems, a semiconductor integrated circuit according to Claim 1 of the present invention includes pads, and wirings which are electrically connected to the pads, wherein said wirings are connected to bumps of a probe card, in an area other than an area where the pads are disposed.

[0008]

Further, according to Claim 2 of the present invention, in the semiconductor integrated circuit defined in Claim 1, at least two of the wirings contact one of the bumps.

[0009]

Further, according to Claim 3 of the present invention, in the semiconductor integrated circuit defined in Claim 2, each of the wirings has a shape having an area that contacts the bump is broader than a linear shape.

[0010]

Further, according to Claim 4 of the present invention, in the semiconductor integrated circuit defined in Claim 2, the wirings have separable portions.

[Effects of the Invention]

[0011]

A semiconductor integrated circuit according to Claim 1 of the present invention includes pads, and wirings which are electrically connected to the pads, wherein said wirings are connected to bumps of a probe card, in an area other than an area where the pads are disposed. Therefore, when executing wafer level burn-in, the chip area of each semiconductor integrated circuit can be reduced without being influenced by the area where the pads are disposed, thereby reducing the cost for chip fabrication.

[0012]

Further, according to Claim 2 of the present invention, in the semiconductor integrated circuit defined in Claim 1, at least two of the wirings contact one of the bumps. Therefore, even when the chip area is reduced, wafer level burn-in can be carried out for all semiconductor integrated circuits on a semiconductor wafer.

[0013]

Further, according to Claim 3 of the present invention, in the semiconductor integrated circuit defined in Claim 2, the wirings have, rather than a linear shape, a shape with an area

where the bump contacts becomes broader. Therefore, an electrode where the bump of the probe card contacts can be secured, thereby improving the contactability.

[0014]

Further, according to Claim 4 of the present invention, in the semiconductor integrated circuit defined in Claim 2, the wirings have separable portions. Therefore, the operation quality of the semiconductor integrated circuit can be secured by only cutting the separable portion after wafer level burn-in. For example, interference of noise that is caused by short-circuiting of the wirings can be avoided.

[Best mode to execute the Invention]

[0015]

(Embodiment 1)

A semiconductor integrated circuit according to a first embodiment of the present invention will be described with reference to figure 4. Figure 4 is a schematic diagram of the semiconductor integrated circuit according to the first embodiment. A plurality of semiconductor integrated circuits shown in figure 4 exist on a semiconductor wafer. The same constituents as those of the semiconductor integrated circuit shown in figure 2 are given the same reference numerals.

[0016]

The semiconductor integrated circuit according to the first embodiment is characterized by that an electrode part is provided

in an area other than the pad area. To be specific, as shown in figure 4, there is provided a wiring 8 which is electrically connected to an area on the pad 4, which area is a bump contact area in the conventional semiconductor integrated circuit. This wiring 8 is contacted to the bump 6 of the probe card 7, and the contact area serves as an electrode part. That is, the bump 6 contacts not the pad 4 but the wiring 8 placed in an area other than the pad area is contacted to the bump 6 to carry out wafer level burn-in. While in figure 4, the electrode part is provided in the empty area in the function circuit 3, the wiring 8 may be provided in any area other than the pad area.

[0017]

The above-mentioned semiconductor integrated circuit according to the first embodiment provides the following effects. In the conventional semiconductor integrated circuit wherein the bump contacts the pad during wafer level burn-in, the chip area depends on the area where the pad is disposed. This is because there is a restriction that a predetermined interval should be secured between adjacent bumps and the pads must be disposed in accordance with the bump interval. Accordingly, the chip area of the semiconductor integrated circuit in which the pads are disposed on the periphery of the function circuit as shown in figure 2 in particular is greatly influenced by the pad area as compared with the function circuit area. Therefore, there are cases where, in the conventional semiconductor integrated circuit,

the chip are cannot be reduced when executing wafer level burn-in. Accordingly, the semiconductor integrated circuit of the first embodiment is provided with the wiring 8 that is electrically connected to the pad 4, and the wiring 8 contacts the bump 6 of the probe card 7 in an area other than the area where the pad 4 is disposed. Thereby, even when executing wafer level burn-in, the chip area of the semiconductor integrated circuit can be reduced without being influenced by the area where the pad is disposed.

[0018]

(Embodiment 2)

Figure 5 is a schematic diagram illustrating the semiconductor integrated circuit according to the second embodiment. As shown in figure 5, the semiconductor integrated circuit is constituted such that at least two wirings 8 simultaneously contact one bump 6. Hereinafter, a description will be given of the case where two wirings (wirings 8a and 8b) contact one bump 6.

[0019]

Figure 6 is an enlarged view of an electrode part 9 that is an area where the wirings 8a and 8b contact the bump 6. As shown in figure 6, the wirings 8a and 8b are disposed so as not to contact each other. And at the same time, the wirings 8a and 8b are disposed to contact the bump 6. The wirings 8a and 8b may have any shape such as a linear shape, a curved shape, or a dot

shape. Preferably, each wiring should have a shape so that an area that contacts the bump 6 is broader than a linear shape,. For example, a vent shape, and a comb-like shape and a whorl-like shape as shown in figures 6 and 7 are preferable. Thereby, the area of the electrode part 9 that is a contact area of the wirings 8 with the bump 6 of the probe card 7 can be secured, thereby to improve contactability.

[0020]

As described above, the semiconductor integrated circuit according to the second embodiment is provided with the wirings 8 which are electrically connected to the pads 4, and at least two wirings 8 and one bump 6 contact each other in an area other than the bump area. Thereby, wafer level burn-in can be carried out with less number of bumps. As a result, it is possible to perform wave level burn-in for all the semiconductor integrated circuits on the semiconductor wafer even when the chip areas of the respective semiconductor integrated circuits are reduced.

[0021]

While in this second embodiment the example where two wirings contact one bump has been described, the present invention is not restricted thereto. The number of wirings contacting one bump may be more than two.

[0022]

(Embodiment 3)

Figure 8 is an enlarged view of an electrode part of the

semiconductor integrated circuit according to the third embodiment. In the semiconductor integrated circuit as shown in figure 8, the shape of a wiring 8 is made such that at least two wirings 8a and 8b and one bump 6 contact simultaneously.

[0023]

As shown in figure 8, the integrated circuit is provided with separable portions 10 between the two wirings 8a and 8b. The separable portions 10 of the wirings 8 are cut, considering that a voltage difference might occur between the wirings 8a and 8b during actual operation after wafer level burn-in. Hereinafter, a description will be given by taking the case where the two wirings 8a, 8b are contacted to the bump 6.

[0024]

For example, the separable portion 10 may be a fuse or a switching element. A fuse is an element that is able to perform only one switching from ON to OFF, as disclosed in Japanese Published Patent Application NO.52-67741(Patent Document No.2). However, even when an area existing as an element cannot be clearly distinguished from other elements and wirings, if switching is possible in that area, it is considered that a fuse is connected to that area. Further, the separable portion 10 is not restricted to a fuse capable of onetime switching operation, and it may be a switching element capable of performing multiple switching.

[0025]

As described above, in the semiconductor integrated circuit according to the third embodiment, the wirings 8 which are electrically connected to the pad 4 are provided, and the separable portions 10 are provided in the wirings 8. Therefore, the operation quality of the semiconductor integrated circuit can be secured during actual operation by only cutting the separable portions 10 after wafer level burn-in. For example, interference of noise that is caused by short-circuiting of the wirings can be avoided.

[Industrial applicability]

[0026]

The present invention is useful as a semiconductor integrated circuit executing burn-in in wafer level.

[Brief description of the Drawings]

[Figure 1]

Figure 1 is a plan view of a semiconductor wafer.

[Figure 2]

Figure 2 is a schematic diagram of a conventional semiconductor integrated circuit.

[Figure 3]

Figure 3 is a diagram illustrating the states of a semiconductor wafer and a probe card during waver level burn-in.

[Figure 4]

Figure 4 is a schematic diagram of a semiconductor integrated circuit according to a first embodiment.

[Figure 5]

Figure 5 is a schematic diagram of a semiconductor integrated circuit according to a second embodiment.

[Figure 6]

Figure 6 is an enlarged view of an electrode part 9 which is an area where wirings 8 contact a bump 6, in the semiconductor integrated circuit according to the second embodiment.

[Figure 7]

Figure 7 is a diagram illustrating examples of shapes of the wirings 8.

[Figure 8]

Figure 8 is an enlarged view of an electrode part 9 which is an area where wirings 8 contact a bump 6, in a semiconductor integrated circuit according to a third embodiment.

[Description of Reference Numerals]

1...semiconductor wafer

2...semiconductor circuit

3...function circuit

4...pad

5...bump contact area

6...bump

7...probe card

8...wiring

9...electrode

10...separable portion

[Name of the Document] Abstract

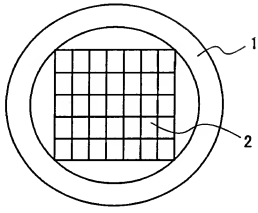
[Summery]

[Object] It is an object to provide a semiconductor circuit which can execute wafer level burn-in even if the chip area thereof is reduced.

[Solution] Each of plural semiconductor integrated circuits existing on a semiconductor wafer is provided with a function circuit 3, plural pads 4, and wirings 8 which are electrically connected to the pads 4 and contact bumps of a probe card 7, wherein at least two wirings 8 simultaneously contact one bump 6 in an area other than a bump area, without being in touch with each other, whereby wafer level burn-in is executed.

[Selected Figure] Figure 5

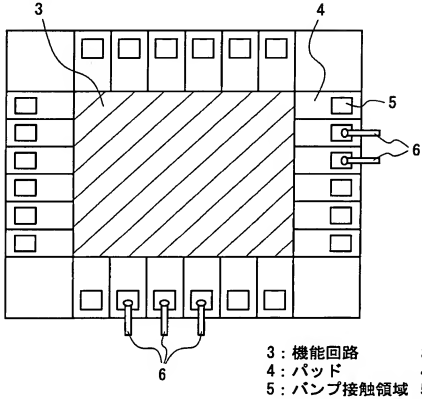
Name of Document
【書類名】　図面 Drawing
【図1】 Figure 1



1：半導体ウェア
2：半導体集積回路

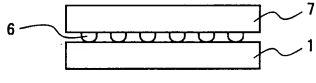
1 : semiconductor wafer
2 : semiconductor circuit

【図2】 Figure 2



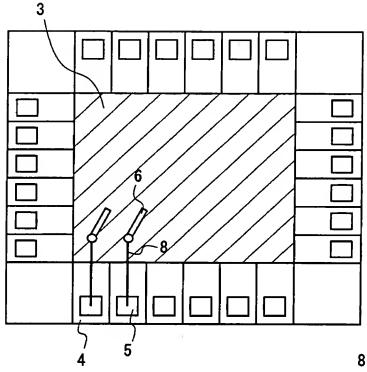
3：機能回路　　3 : function circuit
4：パッド　　4 : pad
5：バンプ接触領域　5 : bump contact area
6：バンプ　　6 : bump

【図3】 Figure 3



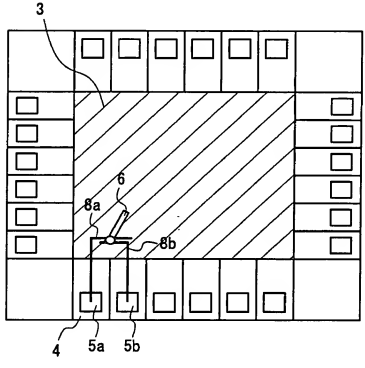
7：プローブカード
7 : probe card

【図4】 Figure 4

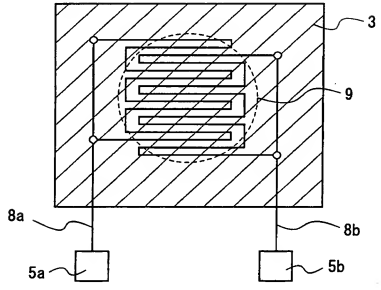


8：配線
8：wiring

【図5】 Figure 5

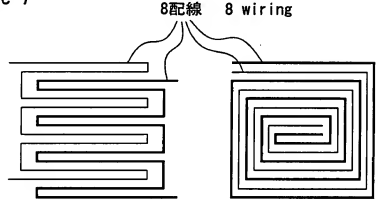


【図6】 Figure 6

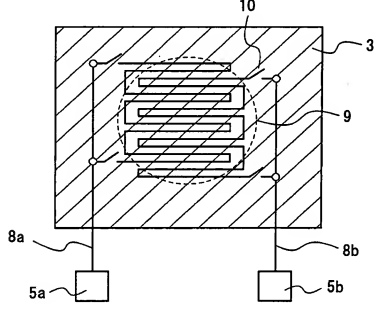


9：電極部
9：electrode

【図7】 Figure 7



【図8】 Figure 8



10：切り離し部
10：separable portion